

REMARKS

The Advisory Action dated October 19, 2006 has been received and carefully noted. Claims 1-31 were examined in the previous Final Office Action dated August 10, 2006. Claims 1-3, 5-11, 13-18 and 20-31 were rejected under 35 U.S.C. § 102(b) and claims 4, 12 and 19 were rejected under 35 U.S.C. § 103(a). In the subsequent Advisory Action, the Examiner stated that the claim amendments in response to the Final Office Action were not entered since the modified claims were too broad.

Applicants note with appreciation the Examiner's assertion in the Advisory Action that the amended drawings have overcome the objections to the drawing that were presented in the Final Office Action.

Claims 1, 9, 17 and 27 are amended and entry is requested. Support for amended claims 1, 9, 17 and 27 can be found in, for example, ¶ [0015]. As such, no new matter has been added. Claims 32-37 remain cancelled. Claims 1-31 remain pending in the application.

Reconsideration of the pending claims is respectfully requested in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. § 102(b)

Claims 1-3, 5-11, 13-18 and 20-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent Pub. No. 2001/0008496 by Leung et al. (hereinafter "*Leung*"). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *MPEP* § 2131. Applicants respectfully submit that each and every element in independent claims 1, 9, 17 and 27, as amended, is not set forth in the cited reference.

Independent claims 1, 9, 17 and 27 have been amended and now include the limitation of "the refresh logic to detect a pattern on the first memory bus to identify a time to carry out the refresh operations." *Leung* describes a memory that must be periodically refreshed (*Abstract*). According to *Leung*, a memory controller includes a refresh manager that monitors the number of idle cycles on the system bus during a refresh period (*Leung, Page 1, Paragraph 10*). Refresh managers 600, 700 and 800 of the various embodiments are each located in the memory

controller (*Page 7, Paragraph 81*). This refresh manager monitors the number of idle cycles on the system bus, and forces one or more idle cycles on the system bus if the monitored number of idle cycles is less than the predetermined number of idle cycle during the refresh period (*Page 1, Paragraph 10*). Thus, in *Leung*, the refresh manager relies only on the number of idle cycles to determine if it is necessary to add any more idle cycles. No other decision factor is used by the refresh manager to optimize the refresh operation. Thus, in contrast to claims 1, 9, 17 and 27, a refresh request according to *Leung* is determined not by monitoring the memory bus for a pattern of behavior on the memory bus but by monitoring idle cycles for a time to carry out refresh operations.

In the Advisory Action, The Examiner in the continuation of Note 3, notes that “the newly claimed ‘pattern’ (which applicant’s remark has characterized as a “pattern of behavior”) is broad enough to include within its scope detecting idle cycles, or a particular number of idle cycle, such as in the *Leung*, because there is no negative limitation in the claims to exclude idle cycles.” Applicants respectfully submit that the word “pattern” is not broad enough to include within its scope detecting or counting of idle cycles.

During patent prosecution, the words used in claims must be accorded their plain meaning unless applicant has provided a clear definition in the specification. *See MPEP § 2111.01*. According to its plain meaning, “pattern” is defined as “[a] consistent, characteristic form, style, or method” (*The American Heritage® Dictionary of the English Language, Fourth Edition*, Houghton Mifflin Company, 2004. <http://dictionary.reference.com/browse/pattern> (accessed: October 25, 2006)). “Characteristic” is defined as “[a] feature that helps to identify, tell apart, or describe recognizably; a distinguishing mark or trait” (*The American Heritage® Dictionary of the English Language, Fourth Edition*, Houghton Mifflin Company, 2004. <http://dictionary.reference.com/browse/characteristic> (accessed: October 25, 2006)). Idle cycles on the memory bus are not a distinguishing mark or trait of a signal on a memory bus since it is merely an absence of a signal. It is not a feature that a person of ordinary skill in this particular art would associate as identifying or telling apart one type of signal from another on a memory bus. As such, detecting idle cycle is not equivalent to “pattern” detection on a memory bus. Further, counting the idle cycles is not equivalent to detecting a “pattern” on the bus. Counting the number of idle cycles does not change that what is detected in *Leung* is not a pattern. Given

this distinction, *Leung* does not disclose the limitation “the refresh logic to detect a pattern on the first memory bus to identify a time to carry out the refresh operations.”

Thus, *Leung* does not include each and every element of independent claims 1, 9, 17 and 27. Claims 2-8, 10-16, 18-26 and 28-31 include all of the limitations of their respective independent claims. Therefore, *Leung* does not anticipate these claims. Accordingly, Applicants respectfully submit that independent claims 1, 9, 17 and 27 and their respective dependent claims are patentable in view of *Leung*.

II. Claims rejected under 35 U.S.C. § 103(a)

Claims 4, 12 and 19 were rejected under 35 U.S.C. § 103(a) as obvious over *Leung* in view of U.S. Patent No. 6,925,086 issued to Curtis (hereinafter “*Curtis*”). To establish a *prima facie* case of obviousness: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference; (2) there must be a reasonable expectation of success; and (3) the references when combined must teach or suggest all of the claim limitations. *MPEP* § 2142. Applicants respectfully submit that a *prima facie* case of obviousness has not been established.

More particularly, the references when combined do not teach or suggest all of the claim limitations of dependent claims 4, 12 and 19. *Curtis* discloses a packet memory system. (*Abstract*). As discussed previously, independent claims 1, 9 and 17 include the limitation of “the refresh logic to detect a pattern on the first memory bus to identify a time to carry out the refresh operations.” Dependent claims 4, 12 and 19 depend from independent claims 1, 9 and 17, respectively.

For the reasons set forth above in regard to independent claims 1, 9 and 17, *Leung* does not teach the elements of claims 1, 9, and 17. *Curtis* does not cure these defects of *Leung*. The Examiner has not relied upon and the Applicants have been unable to discern any part of *Curtis* that discloses these elements of claims 1, 9 and 17. The response to the amendment filed earlier does not identify any new rational for the rejection. Thus, neither *Leung* nor *Curtis* includes the limitations set forth in independent claims 1, 9 and 17, which are limitations included in dependent claims 4, 12 and 19. Accordingly, Applicants respectfully submit that dependent claims 4, 12 and 19 are patentable over *Leung* in view of *Curtis*.

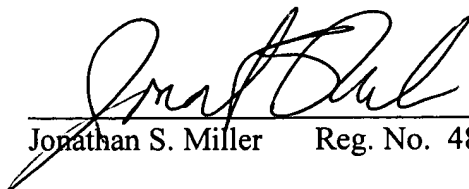
CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1- 31, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

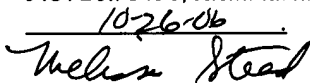
Dated: 10/26, 2006


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